IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2829
Examiner: VELEZ, ROBERTO

In Re PATENT APPLICATION Of:
Applicants : Toshio TERAISHI

Appln. No. : 10 /617,817

Filed : July 14, 2003

For : ANALOG VOLTAGE OUTPUT DRIVER LSI CHIP HAVING TEST CIRCUIT

Attorney Ref. : 03DCOAI030

INFORMATION DISCLOSURE STATEMENT

February 13, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, Va 22313-1450

Sir:

This is an information disclosure statement submitted in compliance with the timing requirements of 37 C.F.R. §1.97(b)(4).

The Examiner's attention is directed to the documents listed on the attached Form PTO-1449. Attached are copies of THREE Japanese laid-open patent publications. The publications are also listed on the attached Form PTO-1449. English abstracts are attached thereto. Each item of information contained in this IDS was first cited in any communication from Japanese patent office in the counterpart Japanese application not more than three months prior to the filing of this IDS. The Notice from Japanese Patent Office is attached hereto with English language translation.

Should any fee be needed, please charge it to our Account No. 50-0945 and advise us accordingly. Consideration of the submitted documents is respectfully requested.

Respectfully submitted,

Junichi Mimura (Reg. No. 40351)
Oki America, Inc.
1101 14th Street N.W., Suite 555
Washington, D.C. 20005
(202) 452-6190
(202) 452-6148 fax
Customer No. 26071

Attachment: Notice from Japanese Patent Office (Original and English Translation)

Date: February 13, 2008